FLOATING POINT DIVIDE AND SQUARE ROOT PROCESSOR

ABSTRACT OF THE DISCLOSURE

An iterative mantissa calculator calculates a quotient mantissa for a divide mode or a result mantissa for a square-root mode. The calculator includes at least first and second summing devices. In the divide mode, each summing device calculates a respective estimated partial remainder W[j+1] for the next iteration, j+1, as $2*W[j]-S_{j+1}*D$, where W[j] is the estimated partial remainder for the current iteration calculated during the prior iteration, S_{j+1} is the quotient bit estimated for the next iteration, and D is the respective divisor bit. The estimated quotient bit for the next iteration is selected based on the calculated partial remainder. In the square-root mode, the first summing device calculates $2W[j]-2S[j]S_{j+1}$, where W[j] is the estimated partial remainder and S_{j+1} is the estimated result generated during the current iteration, j. A shift register shifts the value of the estimated result, S_{j+1}, to generate $-S_{j+1}^2 \bullet 2^{-(j+1)}$, which is summed with the result from the first summing device to generate the estimated partial remainder for the square root mode.